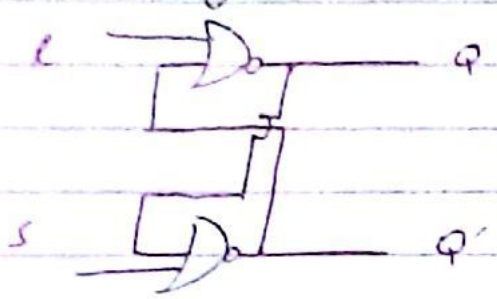
01/02/16

(Lecture 7.8) Latch

- It is simplest Sequential Circuit.

By Nor Gate:-

Diagram of Latch using nor-gate:-



Characteristic Table:-

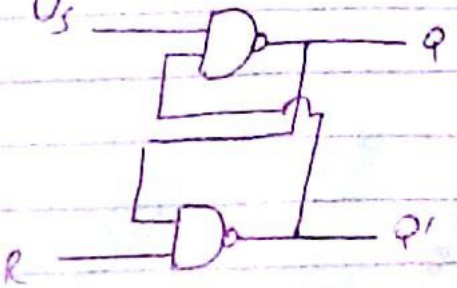
S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	1	0
1	1	0	0

Combinations:-

i) [0,0] Combination is called Memory
ii) [1,0] Combination is called Set.
iii) [0,1] Combination is called Reset.
iv) [1,1] Combination is called Invalid.

By Nand Gate:-

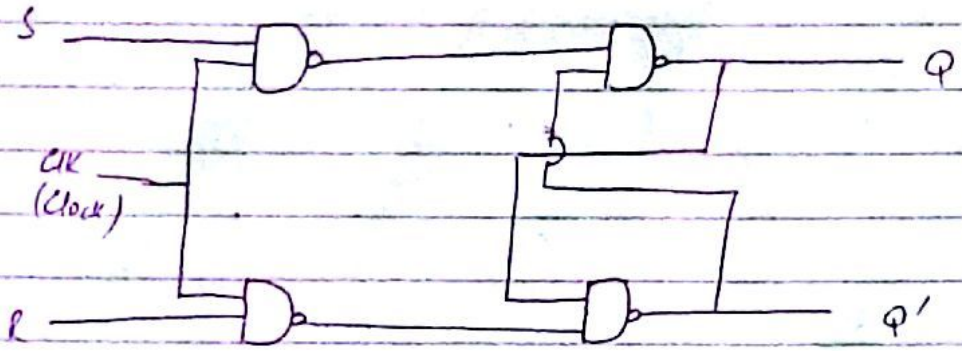
Diagram:-



Characteristic Table

S	R	Q	Q'	
0	0	Invalid		
0	1	1	0	→ Set
1	0	0	1	→ Reset
1	1	Memory		

Clock Latch / S-R Flip Flop



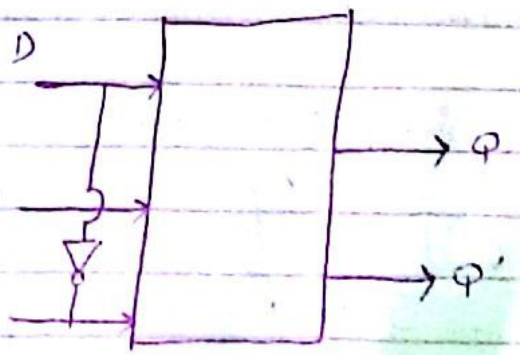
Characteristics Table:-

clk	S	R	Q	Q'
0	x	x	Memory	
1	0	0	"	
1	0	1	0	1
1	1	0	1	0

D - Flip flop :-

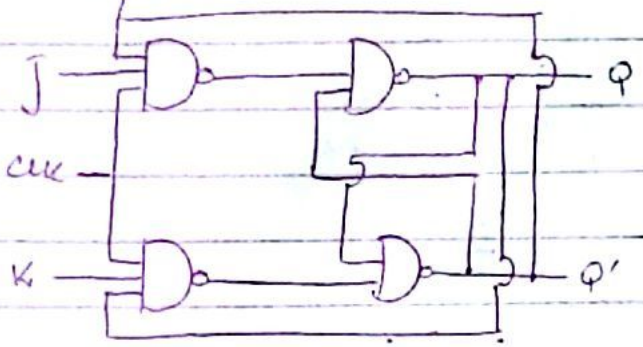
D	Q
0	0
1	1

Block Diagram:-



- It is used in development of Registers.

Clock Locked with Modification -



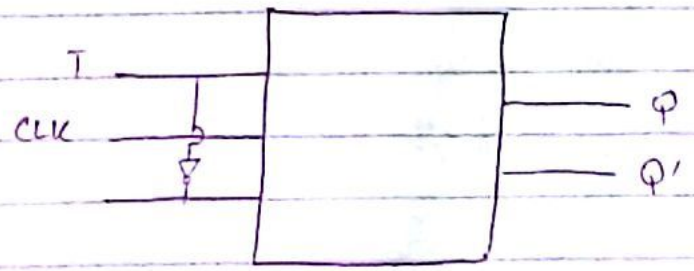
Characteristic Table

CLK	J	K	Q_{n+1}	Q'
0	x	x	Memory	
1	0	0	"	
1	0	1	1	0
1	1	0	0	1
1	1	1	$\bar{Q}_n$	

Toggling will produce in this stage

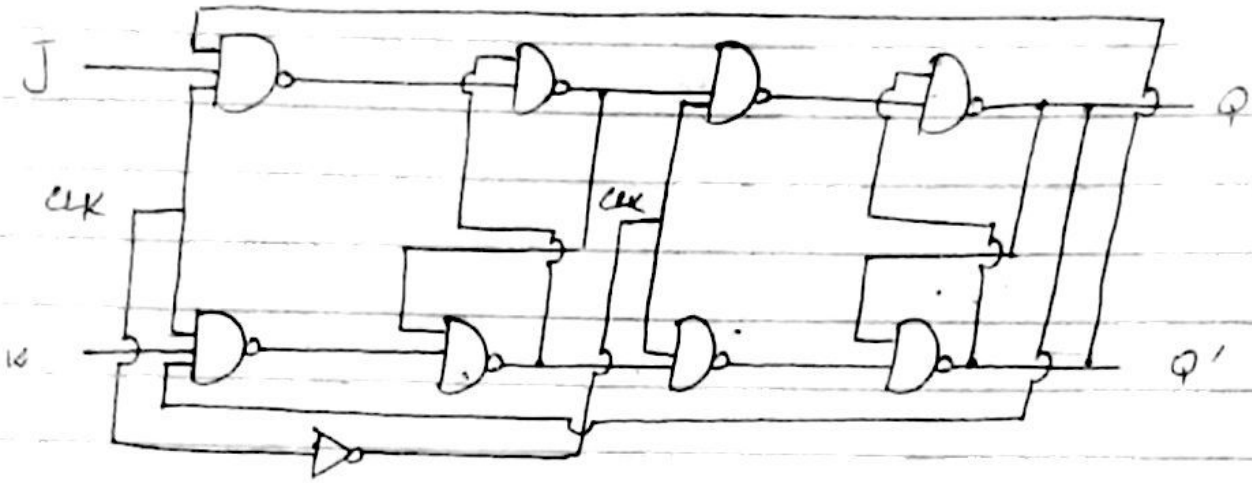
It is called Racing Condition.

Toggling Flip-Flop



- It only saves the data of one bit Q.
- Q' is only the inverse of Q.

Master - Slave Flip - Flop



Edge - Triggered Flip - Flop

- Clock has low and high levels. 
- If we are going from low to high then it is positive edge or vice-versa.

→ Circuits Triggered on positive edge are called positive edge flip-flop.

→ Circuits Triggered on negative edge are called negative edge flip-flop.